DESIGN OF A 32-BIT SPARSE TREE ADDER WITHCARRY SELECT

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ABSTRACT

Now adays general public safety is very important factor as there is lot of increase in number of crimes, attacks against public and thefts all over the world. In such situations we need to take care of the public regarding their safety measures. Here we use high clock speed ARM 7 LPC 2148 microcontroller, RF communication and GSM communication for fast and better response of the system. We are going to use a smart and innovative approach for tracking a person under vulnerable rescue the person by sending SMS to the needy. In additional to that we use LED on and off and buzzer sound to generate alert at the person under threat and also, we use rescuing access modules attached to each street light pole which alerts by LED on and off, buzzer sound and displays message such that a person is in danger on a LCD.

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1. Related work

According to Shubham [1] And Navdeep Prashar2 Parallel prefix adder is used for speeding up the logical operation of the system. Implementation of parallel prefix adder's structure in VLSI have effective performance. The different types of parallel prefix adder structures are Kogge-Stone, Brent-Kung, Sparse Kogge-Stone adder etc. have been proposed previously. Among them Kogge- Stone adder is the fastest adder structure. Sparse Kogge-Stone adder is the sub-type of Kogge-Stone adder in which it uses fewer black cells and grey cells as compared with the Kogge-Stone adder and final sum is calculated through ripple carry adder. In this paper, firstly Basic Sparse Kogge Stone adder is implemented and secondly, implementation of the Sparse Kogge-Stone adder using carry select logic is performed that result in reduction in critical path delay and increase in speed. On verifying its synthesis report it is observed that it requires 72 of its total numbers of slices with minimum path delay of 18.830 ns and a maximum frequency of 53.10 MHz of modified Sparse Kogge-Stone adder. On comparing with Basic Sparse Kingstone adder and previous reference paper, it is observed that the modified design shows the improvement in speed with considerable reduction in delay.

According to A. Padma [2] Priya 32-bit sparse tree adder. In general N-bit adders like Ripple carry adders (slow adders compare to other adders), and carry look ahead adders (area consuming adders) are used in earlier days. But now the most of industries are using parallel prefix adders because of their advantages compare to kogge-stone adder, carry look ahead adder. The prefix sparse tree adders are faster and area efficient. Parallel prefix adder is a technique for increasing the speed in DSP processor while performing addition. We simulate and synthesis different types of 32-bit sparse tree adders using

Xilinx ISE tool, by using these synthesis results, we noted the performance parameters like number of LUT's and delay. We compare these three adders in terms of LUT's represents area) and delay values.

According to Mark A. Anders [3] an adder circuit is provided that includes a propagate and generate circuit stage to provide propagate and generate signals, a plurality of carry-merge stages to provide carry signals based on the propagate and generate signals and a conditional sum generator to provide conditional sums based on the propagate and generate signals. The conditional sum generator includes ripple carry gates and XOR logic gates. The adder circuit also includes a plurality of multiplexers to receive the carry signals and the conditional sums and to provide an output based on the input signals

According to S. Saddam Hussain [4] Arithmetic circuits are the ones which perform arithmetic operations like addition, subtraction, multiplication, division, parity calculation. Most of the time, designing these circuits is the same as designing mixers, encoders and decoders. In electronics, an adder or summer is a digital circuit hat performs addition of numbers. In many computers and other kind of processors, adders are other parts of the processor, many computers and other kinds of processors, where they are used to calculate addresses, table and similar. The binary adder is the one type of element in most digital circuit designs including digital signal processors (DSP) and microprocessor data path units. Therefore, fast and accurate operation of digital system depends on the performance of adders. Hence improving the performance of adder is the main area design.

According to Borkar [5] In this paper, we propose 16-bit sparse tree RSFQ adder (Rapid single flux quantum), kogge-stone adder, carry lookahead adder. In general N-bit adders like Ripple carry adder s (slow adders compare to other adders), and carry lookahead adders (area consuming adders) are used in earlier days. But now the most of industries are using parallel prefix adders because of their advantages compare to kogge-stone adder, carry lookahead adder, our prefix sparse tree adders are faster and area efficient. Parallel prefix adder is a technique for increasing the speed in DSP processor while performing addition. We simulate and synthesis different types of 16-bit sparse tree RSFQ adders using Xilinx ISE10.1i tool, by using these synthesis results, we noted the performance parameters like number of LUT's and delay. We compare these three adders in terms of LUT's represents area) and delay values.

According to Matthew Keeter [6] Ling adders factor complexity out of the first stage of an adder to shorten the critical path. In 2004, Jackson and Talwar proposed a generalization of the Ling adder that reduces the complexity of the critical generate path at the expense of increased complexity in the propagate logic. This paper compares implementations of 32-bit Ling and Jackson adders to the optimized Sklansky architecture produced by Design Compiler in a 45 nm process. The Ling adder is 3% faster and uses 7% less energy, achieving a delay of 8.3 FO4 inverters. The Jackson adder is only 1% faster and uses 45% more energy. However, this is the first published implementation of a Jackson adder with all details shown.

According to M. Varun [7] The two different architectures for adders are introduced in this paper. The first one is built around a sparse carry computation unit that computes only some of the carries of modulo 2n +1 addition. This sparse approach is enabled by the introduction of inverted circular idem potency property of the parallel-prefix carry operator and its regularity and area efficiency are further enhanced by the introduction of a new prefix operator. The resulting diminished-1 adder can be implemented in a smaller area and consume less power compared to all earlier proposals, maintaining a high operation speed. The second adder architecture unifies the design of modulo 2 n +1 adder. Both the adders are derived and compared by using the simulation results.

According to V. Krishna Kumari [8] In various VLSI designs, the adders are frequently used. The most commonly used adder is the Ripple Carry Adder (RCA), which can be implemented by using half adders and full adders. This RCA is a serial adder which is used to perform any number of additions, but it has propagation delay problem due to carry propagation from stage to stage which leads to more delay. To overcome this delay, parallel adders (parallel prefix adders) are preferred as they pre-compute the carry. The parallel prefix adders are KS adder (kogge-stone), SKS adder (sparse kogge-stone), Spanning tree and Brandun adders. These adders are designed and compared by using power and delay constraints. Simulation and Synthesis process is performed on these adders using by Model sim6.4b, Xilinx ISE9.2i.

According to H. K. Hoe [9] parallel-prefix adders (also known as carry tree adders) are known to have the best performance in VLSI designs. However, this performance advantage does not translate directly into FPGA implementations due to constraints on logic block configurations and routing overhead. This paper investigates three types of carry-tree adders (the Kogge-Stone, sparse Kogge-Stone, and spanning tree adder) and compares them to the simple Ripple Carry Adder (RCA) and Carry Skip Adder (CSA). These designs of varied bit-widths were implemented on a Xilinx Spartan 3E FPGA and delay measurements were made with a high-performance logic analyzer. Due to the presence of a fast carry-chain, the RCA designs exhibit better delay performance up to 128 bits. The carry-tree adders are expected to have a speed advantage over the RCA as bit widths approach 256.

According to Chris Martinez [10] Parallel-prefix adders (also known as carry tree adders) are known to have the best performance in VLSI designs. However, this performance advantage does not translate directly into FPGA implementations due to constraints on logic block configurations and routing overhead. This paper investigates three types of carry-tree adders (the Kogge-Stone, sparse Kogge-Stone, and spanning tree adder) and compares them to the simple Ripple Carry Adder (RCA) and Carry Skip Adder (CSA). These designs of varied bit-widths were implemented on a Xilinx Spartan 3E FPGA and delay measurements were made with a high-performance logic analyzer. Due to the presence of a fast carry-chain, the RCA designs exhibit better delay performance up to 128 bits. The carry-tree adders are expected to have a speed advantage over the RCA as bit widths approach 256.

2. INTRODUCTION:

VLSIisanimplementation technology for electronic circuitry, either analog or digital. There are many applicationsofVLSIinday-to-day life, such as microprocessor, memory etc. This technology has made highly sophisticated control system mass-producible and therefore cheap. In digital logic, the inverter is truly the nucleus of all digital designs. Once its operation and properties are clearly understood, designing more intricate structures such as logic gates, adders, multiplexers and microprocessor is greatly simplified. CMOS technology first proposed in the 1960's. CMOS is referred to as complementary-symmetry metal–oxide–semiconductor.The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is drawn when the transistors in the CMOS device are switching between on and off states. CMOS inverter consists of PMOS and NMOS working as complementary switches.

Addition is one of the four elementary operations in mathematics, the other being subtraction, multiplication and division. In digital systems, addition forms the most important operation. This is primarily because we can perform operations like subtraction, multiplication and division using the addition operation. Hence the design of a very fast, accurate and a lower power consumption adder directly results in the increased speed of the device for faster computational purpose as well as an improved life. Apart from the design, the technology we use to design the adder also plays a huge role in the speed and size of the adder. In normal implementation procedure we use the CMOS logic. Additionally, we have Static CMOS, Differential Pass Transistor logic, Lean Integration Pass Transistor logic and Complementary Pass Transistor Logic. These are some of the commonly used technologies out of the many. The Complementary Pass Transistor Logic will help in a great deal in increasing the signal strength at each stage. Also, we will obtain two signals for each entity (one being the complement of the other). The design can be extended to greater bits in pursuit of catering to the needs of the current processors. Also, various other technologies can be integrated together in order to get an overall better result.

3.Objective and Scope:

With rapid development of portable digital applications, the demand for higher speed, compact implementation and low power dissipation is increased.

Full Adder is one of the fastest adders used in the complex data processing to perform fast arithmetic operations.

GDI is a technique for low power design of digital circuits.

GDI reduces power consumption, delay and area of digital circuits, while maintaining low complexity of logic design.

3.1DESIGN OF A 32-BIT SPARSE TREE ADDER:

In the 32-bit radix-2 sparse tree adder, the first stage operation’s input is adjacent to two of the carry generate signal and carry propagation signal. To establish a sparse tree algorithm, weintroduced Gi:j, Pi:j and Point operation.

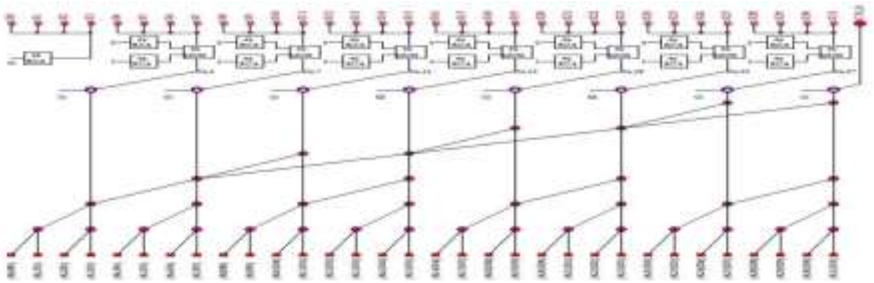

Fig. 3.1 Design of A 32-Bit Sparse Tree adder With Carry Select

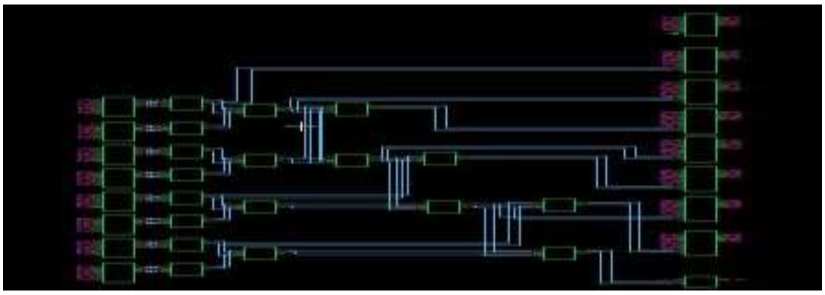

Fig. 3.2 Schematic diagram of A 32-Bit Sparse Tree adder With Carry Select

4. RESULTS:

All the simulations are performed by using Tanner Tool V16.0.

4.1: **Sparse Tree Adder:**

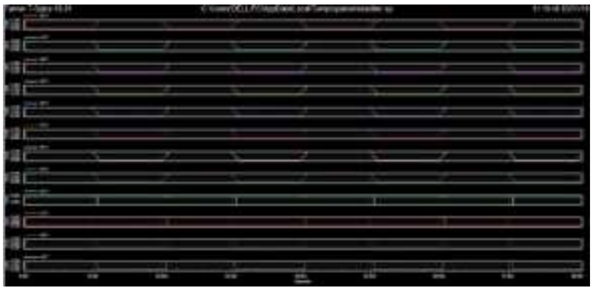

Fig. 4.1 Output wave forms of Sparse Tree Adder with Carry Select

The inputs given in the Sparse tree adder are A=14(0111) and B=15(1111). We get the sum output as S=29(11101) and Carry=1.

5. CONCLUSION:

Sparse Tree Adder increases the speed of arithmetic operations of the system.

The simulation and synthesis of 32-bit Sparse Tree adder have been performed on Tanner tool.

On comparing with Sparse Tree Adder using GDI Technique and basic Sparse Tree Adder, it is observed that modified design shows the improvement in speed with considerable reduction in delay.

So, the modified Sparse Tree Adder can be used for high-speed applications.

6. References:

[1] Shubham1 And Navdeep Prashar2 Volume 3, Issue-5 (September-Octobe2015),

[2] A.Padma Priya1 M.Prem kumar2 Comparative design of 32-bit wave pipelining sparse tree adder[3] Mark A. Anders, Sparse tree adder circuit,

[4] S. SaddamHussain, S. Mahaboob, Comparative Design of 16-Bit Sparse-Tree Rsfq AdderISSN : 2248-9622, Vol. 4, Issue 6(Version 6), June 2014, pp.184-18

[5] Borkar, ―A 4-GHz 130-nm address generation unit with 32-bit sparse-tree adder core,‖ IEEEJ. Solid-State Circuits, vol. 38, no. 5, pp. 689–695, May 2003.

[6] Implementation of 32-bit Ling and Jackson Adders Matthew Keeter, David Money Harris, Andrew Macrae, Rebecca Glick, Madeleine Ong, and Justin Schauer* Harvey Mudd College 301 Platt Blvd. Claremont, CA 91711 {Matthew_Keeter, David_Harris}@hmc.edu * Oracle Redwood Shores.

[7] Design of High Speed Modulo 2 n +1 Adder, M.Varun, M. Nagarjuna, M. Vasavi Volume 81 – No 17, November 2013

[8] V. Krishna Kumari, Y. Sri Chakrapani, Dr. M. Kamaraju, Volume 4, Issue 10, October-2013 1502 ISSN 2229-5518 IJSER © 2013 http://www.ijser.orgDesignand Characterization of Koggestone, Sparse Koggestone, Spanning tree and Brentkung Adders

[9] H. K. Hoe, Sri Jyothsna Vundavalli Design and Characterization of Parallel Prefix Adders usingFPGAsDavidDepartment ofElectrical Engineering The University of Texas, Tyler dhoe@uttyler.edu

[10] Chris Martinez, H. K. Hoe, Sri Jyothsna Vundavalli, Design and Characterization of Parallel Prefix Adders using FPGAs David Department of Electrical Engineering The University of Texas